

# CONTENTS

## **UNIT I: NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES**

**1.1 – 1.56**

<b>Digital Electronics</b>	<b>1.1</b>
<b>1.1. Number Systems</b>	<b>1.2</b>
<b>1.2. Arithmetic Operations</b>	<b>1.12</b>
1.2.1. Binary Addition	1.12
1.2.2. Binary Subtraction	1.13
1.2.3. Binary Multiplication	1.14
1.2.4. Binary Division	1.15
<b>1.3. Complements</b>	<b>1.15</b>
1.3.1. 1's Complement	1.15
1.3.2. 1's Complement Arithmetic	1.16
1.3.3. 2's Complement	1.18
1.3.4. 2's Complement Arithmetic	1.18
1.3.5. 9's Complements	1.21
1.3.6. 9's Complement Arithmetic	1.22
1.3.7. 10's Complement	1.23
1.3.8. 10's Complement Arithmetic	1.24
<b>1.4. Error Detection and Correction</b>	<b>1.25</b>
1.4.1. Hamming Code	1.26
1.4.2. Single Error correction, Double-Error Detection	1.29
<b>1.5. Digital Logic Circuits</b>	<b>1.30</b>
1.5.1. Classification of Digital Logic Families	1.30
1.5.2. Characteristics of Digital ICs	1.31
1.5.3. Resistor-Transistor Logic (RTL)	1.35
1.5.4. Transistor-Transistor Logic (TTL)	1.36
1.5.4.1. TTL Series and their CHARACTERISTICS	1.36

1.5.4.2.	Transistor Configuration of Standard TTL Circuit	1.38
1.5.4.3.	Two-Input TTL NAND Gate	1.38
1.5.4.4.	Three-Input TTL NAND Gate	1.40
1.5.4.5.	Output Configuration of TTL Gates	1.41
1.5.4.6.	Open-Collector Output Gate	1.41
1.5.4.7.	Totem-Pole Output	1.45
1.5.4.8.	Schottky TTL Gate	1.47
<b>1.5.5.</b>	<b>Emitter-Coupled Logic (ECL)</b>	<b>1.49</b>
<b>1.5.6.</b>	<b>Complementary Metal Oxide Semiconductor (CMOS)</b>	<b>1.51</b>
1.5.6.1.	Operation of Inverter	1.52
1.5.6.2.	CMOS NAND Gate	1.52
1.5.6.3.	CMOS-NOR Gate	1.53
1.5.6.4.	MOS Transistor Electronic Switch	1.54
1.5.6.5.	CMOS Inverter Switch Model	1.54
1.5.6.6.	CMOS Inverter Logical Model	1.54
1.5.6.7.	CMOS Characteristics	1.55
<i>Two Mark Questions and Answers</i>		<b>1.56</b>
<i>Review Questions – Part B</i>		<b>1.56</b>

**UNIT II: COMBINATIONAL CIRCUITS****2.1 – 2.178**

<b>2.1.</b>	<b>Boolean Algebra</b>	<b>2.1</b>
2.1.1.	Postulates of Boolean Algebra	2.1
2.1.2.	Laws of Boolean Algebra	2.2
2.1.3.	DeMorgan's Theorems	2.5
2.1.4.	Duality Theorem	2.5
2.1.5.	Basic Theorems	2.6
2.1.6.	Consensus Theorem	2.8
<b>2.2.</b>	<b>Boolean Expression</b>	<b>2.9</b>
2.2.1.	Minterms	2.10

2.2.2.	Maxterms	2.10
2.2.3.	Sum of Product Terms (SOP)	2.11
2.2.4.	Product of Sum Terms (POS)	2.11
2.3.	<b>Standard SOP and POS Forms</b>	<b>2.12</b>
2.3.1.	Converting SOP to Standard SOP Form	2.13
	<i>Exercise Problem</i>	<b>2.14</b>
2.3.2.	Converting POS to Standard POS Forms	2.15
	<i>Solved Examples</i>	<b>2.15</b>
	<i>Exercise Problem</i>	<b>2.16</b>
2.4.	<b>Minimization of Boolean Expression</b>	<b>2.16</b>
	<b>Examples for Minimization of Boolean Expression</b>	<b>2.17</b>
	<i>Exercise Problems</i>	<b>2.19</b>
2.4.1.	Karnaugh Map Minimization (K-Map)	2.23
	<i>Solved Examples</i>	<b>2.31</b>
	<i>Exercise Problems</i>	<b>2.38</b>
	Minimization of POS Form	2.38
	<i>Exercise Problem</i>	<b>2.44</b>
2.4.2.	Don't Care Condition	2.45
	<i>Exercise Problem</i>	<b>2.49</b>
	Five Variable K-Map	2.50
	<i>Exercise Problem</i>	<b>2.53</b>
2.4.3.	Quine–McCluskey	2.53
	<i>Exercise Problem</i>	<b>2.64</b>
	<i>Solved Examples</i>	<b>2.64</b>
	<i>Exercise Problem</i>	<b>2.68</b>
2.5.	<b>Digital Logic Gates</b>	<b>2.68</b>
2.5.1.	Universal Gates	2.73
2.6.	<b>Implementation of Logic Functions using Gates</b>	<b>2.79</b>
	<i>Solved Examples</i>	<b>2.79</b>

2.6.1.	NAND-NAND Implementation	2.81
	<i>Solved Examples</i>	<b>2.82</b>
2.6.2.	NOR-NOR Implementation	2.83
	<i>Solved Examples</i>	<b>2.84</b>
	<i>Exercise Problems</i>	<b>2.88</b>
2.7.	<b>Design Procedure</b>	<b>2.89</b>
	<i>Solved Examples</i>	<b>2.89</b>
	<i>Exercise Problem</i>	<b>2.98</b>
2.8.	<b>Binary Adder – Subtractor</b>	<b>2.98</b>
2.8.1.	Half Adder	2.98
2.8.2.	Full Adder	2.99
2.8.3.	Half Subtractor	2.102
2.8.4.	Full Subtractor	2.102
2.8.5.	Parallel Adder	2.105
2.8.6.	Parallel Subtractor	2.107
	<i>Solved Example</i>	<b>2.108</b>
2.8.7.	Adder/Subtractor	2.108
2.9.	<b>Carry Look Ahead Adder (Fast Adder)</b>	<b>2.109</b>
2.10.	<b>Serial Adder/Subtractor</b>	<b>2.113</b>
2.11.	<b>BCD Adder</b>	<b>2.114</b>
2.12.	<b>Binary Multiplier</b>	<b>2.117</b>
2.13.	<b>Binary Divider</b>	<b>2.120</b>
2.14.	<b>Multiplexers</b>	<b>2.121</b>
2.14.1.	4 to 1 Multiplexer	2.122
2.14.2.	8 to 1 Multiplexer	2.123
2.14.3.	Implementation of Boolean Function using Multiplexer	2.125
2.15.	<b>Demultiplexer</b>	<b>2.127</b>
2.15.1.	1 to 4 Demultiplexer	2.128
2.15.2.	1 to 8 Demultiplexer	2.129

<b>2.16. Decoder</b>	<b>2.130</b>
2.16.1. Binary to Octal Decoder (3 to 8 Decoder)	2.131
2.16.2. BCD to Decimal Decoder	2.132
2.16.3. BCD to Seven Segment Decoder	2.134
<b>2.17. Encoders</b>	<b>2.140</b>
2.17.1. Octal to Binary Encoder	2.140
2.17.2. Priority Encoder	2.141
<b>2.18. Parity Generator and Checker</b>	<b>2.143</b>
<b>2.19. Code Converters</b>	<b>2.146</b>
2.19.1. Binary to BCD Converters	2.146
2.19.2. BCD to Binary Converters	2.149
2.19.3. BCD to Excess-3 Code Converter	2.152
2.19.4. Excess 3 to BCD Code Converter	2.154
2.19.5. Binary to Gray Code Converter	2.156
2.19.6. Gray Code to Binary Code Converter	2.158
<b>2.20. Magnitude Comparator</b>	<b>2.161</b>
<i>Solved Examples</i>	<b>2.166</b>
<i>Two Mark Questions and Answers</i>	<b>2.168</b>
<i>Review Questions – Part B</i>	<b>2.177</b>

---

**UNIT III: SYNCHRONOUS SEQUENTIAL CIRCUITS****3.1 – 3.135**

<b>3.1. Latches</b>	<b>3.3</b>
3.1.1. Gated SR Latch	3.3
3.1.2. Gated D Latch	3.6
<b>3.2. Flip-Flops</b>	<b>3.7</b>
3.2.1. Triggering of Flip-flops	3.7
3.2.2. Clocked SR Flip-Flop	3.10
3.2.3. D-Flip-Flop	3.13

3.2.4.	JK Flip-Flop	3.15
3.2.5.	T Flip-Flop	3.18
3.2.6.	Edge Triggered JK Flip-Flop	3.20
3.2.7.	Master-Slave JK Flip-Flop	3.22
<b>3.3.</b>	<b>Conversion of Flip-Flops</b>	<b>3.24</b>
3.3.1.	SR Flip-Flop to D Flip-Flop	3.24
3.3.2.	SR Flip-Flop to JK Flip-Flop	3.25
3.3.3.	SR Flip-Flop to T Flip-Flop	3.26
3.3.4.	JK Flip-Flop into a D Flip-Flop	3.27
3.3.5.	D Flip-Flop into a JK Flip-Flop	3.28
3.3.6.	D Flip-Flop into a T Flip-Flop	3.29
3.3.7.	JK Flip-Flop into T Flip-Flop	3.30
3.3.8.	JK Flip-Flop to SR Flip-Flop	3.31
<b>3.4.</b>	<b>Counters</b>	<b>3.32</b>
<b>3.5.</b>	<b>Asynchronous (or) Ripple Counter</b>	<b>3.33</b>
3.5.1.	Asynchronous (or) Ripple Up Counter	3.33
3.5.2.	Asynchronous Down Counter	3.36
3.5.3.	Asynchronous Up/Down Counter	3.37
<b>3.6.</b>	<b>Synchronous Counter</b>	<b>3.40</b>
3.6.1.	Synchronous Up Counter	3.40
3.6.2.	Synchronous Down Counter	3.43
3.6.3.	Synchronous Up/Down Counter	3.44
<b>3.7.</b>	<b>Decade Counter</b>	<b>3.47</b>
<b>3.8.</b>	<b>Modulo-n Counter</b>	<b>3.48</b>
3.8.1.	Design a Synchronous Mod-6 Counter using Clocked JK Flip-Flop	3.48
3.8.2.	Design a Synchronous Mod-11 Counter using Clocked D-Flip-Flop	3.50
3.8.3.	Design a Synchronous Mod-5 Counter using T-Flip-Flop	3.54
3.8.4.	Design of a Synchronous Mod-6 Counter Using Clocked SR Flip-Flop	3.55
	<b>Solved Examples</b>	<b>3.57</b>

3.8.5. Design a Mod-8 Synchronous Up/Down Counter	3.59
<b>3.9. Classification of Synchronous Sequential Circuits</b>	<b>3.61</b>
<b>3.10. Analysis of Clocked Sequential Circuit</b>	<b>3.62</b>
<b>3.11. Design of Clocked Sequential Circuits</b>	<b>3.65</b>
3.11.1. State Minimization (or) State Reduction Techniques	3.71
<i>Solved Examples</i>	<b>3.73</b>
3.11.2. State Assignment	3.77
<i>Exercise Problem</i>	<b>3.100</b>
<b>3.12. Sequence Generator</b>	<b>3.101</b>
3.12.1. Sequence Generator using Counters	3.101
3.12.2. Sequence Generator using Shift Register	3.102
<b>3.13. Sequence Detector</b>	<b>3.103</b>
<i>Exercise Problems</i>	<b>3.112</b>
<b>3.14. Registers</b>	<b>3.113</b>
3.14.1. Register with Parallel Load	3.114
<b>3.15. Shift Registers</b>	<b>3.116</b>
3.15.1. Serial In Serial Out Shift Register	3.116
3.15.2. Serial In Parallel Out Shift Register	3.119
3.15.3. Parallel In Serial Out Shift Register	3.119
3.15.4. Parallel In Parallel Out Shift Register	3.121
3.15.5. Universal Shift Register	3.122
<b>3.16. Shift Register Counters</b>	<b>3.125</b>
3.16.1. Ring Counter	3.125
3.16.2. Johnson Counter	3.126
<i>Two Marks Questions and Answers</i>	<b>3.128</b>
<i>Review Questions</i>	<b>3.135</b>

**UNIT IV: ASYNCHRONOUS SEQUENTIAL CIRCUITS AND  
PROGRAMMABILITY LOGIC DEVICES**

4.1 – 4.92

<b>4.1.</b>	<b>Analysis of Pulse Mode Asynchronous Sequential Circuit</b>	<b>4.1</b>
<b>4.2.</b>	<b>Design of Pulse Mode Asynchronous Sequential Circuit</b>	<b>4.6</b>
	<i>Solved Examples</i>	<b>4.7</b>
<b>4.3.</b>	<b>Analysis of Fundamental Mode Asynchronous Sequential Circuit</b>	<b>4.12</b>
<b>4.4.</b>	<b>Cycles and Races Conditions</b>	<b>4.15</b>
4.4.1.	Shared Row State Assignment	4.17
4.4.2.	One Hot State Assignment	4.19
<b>4.5.</b>	<b>Design of Fundamental Mode Asynchronous Sequential Circuits</b>	<b>4.20</b>
	<i>Solved Examples</i>	<b>4.21</b>
<b>4.6.</b>	<b>Hazards</b>	<b>4.49</b>
4.6.1.	Static Hazards	4.49
4.6.2.	Dynamic Hazards	4.53
	<i>Solved Examples</i>	<b>4.54</b>
<b>4.7.</b>	<b>Essential Hazards</b>	<b>4.55</b>
	<i>Solved Examples</i>	<b>4.57</b>
<b>4.8.</b>	<b>Programmable Logic Devices (PLDs)</b>	<b>4.58</b>
4.8.1.	Types of PLDs	4.58
4.8.2.	Programmable Logic Array (PLA)	4.61
	<i>Solved Examples</i>	<b>4.62</b>
4.8.3.	Programmable Array Logic (PAL)	4.69
	<i>Solved Examples</i>	<b>4.70</b>
<b>4.9.</b>	<b>Field Programmable Gate Array (FPGA)</b>	<b>4.79</b>
4.9.1.	Architecture of Xilinx FPGA's	4.79
4.9.2.	Application of FPGA	4.83
<b>4.10.</b>	<b>Application Specific Integrated Circuits (ASIC)</b>	<b>4.84</b>
	<i>Two Mark Questions and Answers</i>	<b>4.85</b>
	<i>Exercise Problems</i>	<b>4.91</b>
	<i>Review Questions</i>	<b>4.91</b>



<b>UNIT V: VHDL</b>	<b>5.1 – 5.94</b>
5.1. Introduction	5.1
5.2. Architecture	5.5
5.3. Operators	5.7
5.4. Packages	5.9
5.5. Data Types	5.13
5.5.1. Defining Signals	5.13
5.6. Process	5.17
5.7. VHDL Sequential Statements	5.23
5.8. VHDL Concurrent Statements	5.32
5.9. Functions	5.42
5.10. Procedures	5.43
5.11. Simulation	5.45
5.12. RTL Design	5.48
5.12.1. RTL Design Example	5.51
5.13. Simulation and Tutorial Examples	5.53
<i>Two Marks Questions and Answers</i>	5.90
<i>Review Questions – Part B</i>	5.94

SOLVED ANNA UNIVERSITY QUESTIONS PAPERS

