

ANALOG IC DESIGN

CEC 334 (Professional Elective - I)

Vertical - I, Semi Conductor Chip and Design

For B.E. V / VI Semester ECE Branch

**As per the Latest Syllabus of Anna University, Chennai
(Regulations - 2021)**

**QUALITY
WITH
LOW PRICE
EDITION**



**With Latest Solved Anna University
Question Paper Nov / Dec 2023**



**Dr. B. BALRAJ
Dr. D. SIVA SUNDHARA RAJA**

**LAKSHMI PUBLICATIONS
CHENNAI**

SYLLABUS

ANNA UNIVERSITY, CHENNAI

For B.E., Electronics and Communication Engineering Branch

CEC 334

ANALOG IC DESIGN

L T P C

2023

UNIT I: Single Stage Amplifiers

6

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers - to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II: High Frequency and Noise Characteristics of Amplifiers

6

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III: Feedback and Single Stage Operational Amplifiers

6

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV: Stability, Frequency Compensation

6

Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two Stage Op Amps, Slewing in Two Stage Op Amps, Other Compensation Techniques.

UNIT V: Logic Circuit Testing

6

Faults in Logic Circuits - Basic Concepts of Fault Detection - Design for Testability - Ad Hoc Techniques, Level - Sensitive Scan Design, Partial Scan, Built-in Self-Test.

30 PERIODS

CONTENTS

UNIT I

SINGLE STAGE AMPLIFIERS	1.1 - 1.114
1.1. Basic MOS Device Physics and Equivalent Circuits and Models.....	1.1
1.1.1. General Considerations	1.1
1.1.2. MOS I/V Characteristics	1.3
1.1.3. Second-Order Effects.....	1.7
1.1.4. MOS Device Models.....	1.9
1.1.5. FinFETs.....	1.14
1.1.6. Behavior of a MOS Device as a Capacitor	1.16
1.2. Common Source Stage.....	1.17
1.2.1. Low Frequency behavior of the Circuit	1.18
1.2.2. Common Source Stage with Diode Connected Load.....	1.20
1.2.3. Common Source Stage with Current Source Load	1.22
1.2.4. Common Source Stage with Triode Load.....	1.23
1.3. Common-Gate Configuration.....	1.23
1.3.1. Common-Gate Input Resistance	1.25
1.3.2. Common Gate Output Resistance	1.26
1.4. Common-Drain Configuration (Source Follower).....	1.28
1.5. Differential Amplifier with Active Load.....	1.30
1.5.1. Single Ended and Differential Operation	1.30
1.5.2. Basic Differential Pair.....	1.32
1.5.3. Differential Pair with Loads.....	1.44
1.6. Cascode and Folded Cascode Configuration.....	1.46
1.6.1. Need for the Cascode Configuration.....	1.46
1.6.2. Cascode configuration for MOSFETs.....	1.47
1.7. Design of Differential Amplifier	1.50

1.7.1. Characterization of a Differential Amplifier.....	1.50
1.8. Design of Cascode Amplifiers	1.72
Problems	1.91
Two Mark Questions and Answers	1.108
Review Questions	1.114

UNIT II

HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS 2.1 - 2.56

2.1. Miller Effect.....	2.1
2.1.1. Signal-Stage Voltage Amplifiers and The Miller Effect.....	2.1
2.1.2. Small-Signal Model Elements.....	2.2
2.1.3. The MOS Differential Amplifier: Differential-Mode Gain	2.8
2.2. Frequency Response of the Common-Mode Gain for a Differential Amplifier ..	2.10
2.3. Variation with Frequency of the Gain Parameters for the Differential Amplifier	2.12
2.4. Frequency Response of the Source Follower.....	2.13
2.5. Common-Gate Amplifier Frequency Response	2.13
2.6. Cascade Voltage-Amplifier Frequency Response	2.15
2.6.1. Cascode Frequency Response	2.15
2.6.2. Cascode Differential Amplifier.....	2.17
2.7. Frequency Response of a Current Mirror Loading a Differential Pair.....	2.18
2.8. Statistical Characteristics of Noise	2.21
2.8.1. Noise Spectrum	2.23
2.8.2. Amplitude Distribution	2.26
2.8.3. Correlated and Uncorrelated Sources.....	2.27
2.9. Noise in Single-Stage Amplifiers.....	2.28
2.9.1. Common Source Stage.....	2.29
2.9.2. Common Gate Stage	2.30
2.9.3. Source followers	2.32

2.9.4. Cascode Stage	2.33
2.10. Noise in Differential Pairs	2.34
Problems	2.37
Two Mark Questions and Answers	2.52
Review Questions	2.56

UNIT III

FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS 3.1 - 3.43

3.1. Concept of Negative Feedback.....	3.1
3.1.1. General Properties of Negative Feedback Systems.....	3.1
3.2. Effects of Loading in Feedback Network.....	3.3
3.2.1. Two-Port Networks Models.....	3.3
3.2.2. Effect of Loading in Voltage-Voltage Feedback	3.4
3.2.3. Effect of Loading in Current-Voltage Feedback.....	3.7
3.2.4. Effect of Loading in Voltage-Current Feedback.....	3.8
3.2.5. Effect of Loading in Current-Current Feedback	3.10
3.2.6. Summary of Loading Effects	3.11
3.3. Operational Amplifier Performance Parameters	3.12
3.3.1. Performance Parameters.....	3.12
3.3.1.1. Input Offset Voltage.....	3.12
3.3.1.2. Input Common Mode Voltage Range.....	3.15
3.3.1.3. Differential Input Voltage Range	3.16
3.3.1.4. Maximum Output Voltage Swing	3.16
3.3.1.5. Large Signal Differential Voltage Amplification.....	3.17
3.3.1.6. Input Parasitic Elements	3.17
3.3.1.7. Output Impedance	3.18
3.3.1.8. Effect of Output Impedance	3.19
3.3.1.9. Common Mode Rejection Ratio	3.19
3.3.1.10. Supply Voltage Rejection.....	3.19

3.3.1.11. Supply Current Rejection	3.20
3.3.1.12. One-stage Op Amps	3.20
3.3.2. Two-Stage Op Amps.....	3.22
3.3.2.1. Input Range Limitations.....	3.25
3.3.2.2. Gain Boosting.....	3.26
3.3.3. Slew Rate	3.29
3.3.4. Power Supply Rejection Ratio (PSRR).....	3.30
3.3.4.1. Power Supplies and Power Dissipation.....	3.32
3.3.4.2. Power Supplies and Decoupling.....	3.33
3.3.5. OpAmp Noise	3.34
3.3.5.1. Op Amp Input Voltage Noise.....	3.34
3.3.5.2. Resistor Noise.....	3.35
3.3.5.3. Op Amp Input Current Noise	3.35
3.3.5.4. Combining Noise Sources.....	3.36
3.3.5.5. Frequency Characteristics of Voltage and Current Noise	3.36
3.3.5.6. Popcorn Noise	3.38
Two Mark Questions and Answers	3.39
Review Questions	3.43

UNIT IV

STABILITY, FREQUENCY COMPENSATION	4.1 - 4.35
4.1. General Considerations	4.1
4.2. Multi-Pole systems	4.4
4.2.1. Construction of Root Locus for a Two-Pole System	4.5
4.3. Phase Margin.....	4.7
4.4. Frequency Compensation.....	4.10
4.4.1. Design of Op-Amp by Poles Minimization.....	4.10

4.4.2. Compensation of Op-Amp	4.10
4.5. Compensation of Two-Stage Op-Amps.....	4.16
4.6. Slewinq in Two Stage of Amps.....	4.23
4.7. Other Compensation Techniques	4.24
Problems	4.29
Two Mark Questions and Answers	4.31
Review Questions	4.35

UNIT V

LOGIC CIRCUIT TESTING	5.1 - 5.30
5.1. Faults at Logic Circuits	5.1
5.2. Basic Concepts of Fault Detection.....	5.7
5.2.1. Stuck-at Faults.....	5.7
5.2.2. Short-Circuit and Open-Circuit Faults	5.8
5.2.3. Observability	5.10
5.2.4. Controllability	5.10
5.2.5. Repeatability	5.11
5.2.6. Survivability.....	5.11
5.2.7. Fault Coverage	5.11
5.2.8. Automatic Test Pattern Generation (ATPG).....	5.11
5.2.9. Delay Fault Testing.....	5.12
5.3. Design for Testability.....	5.13
5.4. AD HOC Approach	5.14
5.4.1. Test Point Insertion	5.15
5.5. Structured Approach.....	5.16
5.6. Level-Sensitive Scan Design (LSSD)	5.18
5.7. Partial Scan	5.19
5.8. Built- in Self-Test (BIST).....	5.23
Two Mark Questions and Answers	5.26
Review Questions	5.30
Solved Anna University Question Paper.....	SQ.1 - SQ.